This paper presents a field programmable gate array (FPGA) based modulator for power factor correction (PFC), applied to a reduced AC-DC matrix converter. The control algorithm has been performed using a hardware description language (VHDL), which provides great flexibility and technology independence. Additional control of the output current is performed on a powerful digital-signal-processor (DSP). The three-phase to one-phase or reduced AC-DC matrix converter consists on an array of six bidirectional switches that are used to connect each input phase to each output phase, without intermediate storage elements. For this power rectifier, the space vector modulation technique (SVM) has been selected, to build a sinusoidal current at the input in phase with the main voltages (PFC). The modulator generates the gate control signal for all power converter switches, according to SVM technique.

Additional commutation hazards occur with these bi-directional switches when current commutates from one switch to another. The SVM technique together with the safe-commutation algorithm where implemented in an XCS20XL FPGA by Xilinx. Basically consists on 16 pulse-width-modulator (PWM) generators, where the duty cycles are the sinus function of the SVM technique. Only one counter implements these PWM generators with a clock frequency of 40 MHz, which is high enough for the required duty cycle accuracy.

The FPGA modulator enables two control signals to be changed externally by the DSP, i.e. the modulation index that regulates the output current and the displacement factor that controls the power factor correction. Also it generates two synchronisation signals with the DSP, that are the main synchronisation signal IRQA that inform on the beginning of the switching period and IRQB synchronised with the zero-crossing of the input phase to inform the DSP about the change on the input phase sector. Both FPGA and DSP are included in the same digital card, which allows for compact and good noise immunity design.

Simulation and experimental results show the feasibility of the proposed digital modulator.