ADAPTATION AND AUTOMATION OF THE FPGA DESIGN FLOW FOR ASYNCHRONOUS CIRCUIT IMPLEMENTATION

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Abstract

Nowadays the design of synchronous digital circuits has four main problems:

1. Clock Skew. Microprocessors dedicate a great part of the silicon area for clock signal controllers, and hence the integrated circuit size grows.

2. Power consumption: This grows due to the increase in the number of transistors and also because of the high frequencies used in today’s processors.

3. Electromagnetic compatibility (EMC): microwave radiation which exists during voltages transitions due to the high frequencies, can damage the device. This emission can also produce interferences with the rest of components of the circuit.

4. Errors: Due to the advances in technology is absolutely necessary a fault tolerant design system.

Asynchronous design can provide a solution to the problems explained on the last paragraph. Those circuits work using a communication protocol instead of the usual clock, so clock skew problems disappear because there is not a global clock signal that marks the synchronism of the circuit. Power consumption can also be reduced because with an asynchronous design there are phases in which the circuit does not make any calculation. Fault tolerant design is more effective because the computing or working time is adapted in a dynamic way. Finally, microwave emission is not as bad as in the synchronous case because the spectrum is flatter. In addition, the completion time of an asynchronous circuit is the average case instead of the worst case of the synchronous model. This represents an increase in the performance.

Obviously, asynchronous design also present some disadvantages. For example, it increases the area due to the implementation of a communication protocol and power consumption is higher during synchronization phases because there is more area and more number of transition with the communication protocol. In the design of asynchronous circuits the sum of both power consumptions, during synchronism and computation, must be lower than power consumption of the synchronous circuits. Those are general disadvantages of any asynchronous circuit. One of the main problems of asynchronous design is the lack of automation design tools and environments. The aim of this paper is to present a method to adapt and automate the design flow for FPGAs (Field Programmable Gate Arrays) for asynchronous circuits implementation. The adaptation that proposed this work consists of the creation of a synthesizable standard library of basic asynchronous logic gates, designed in VHDL hardware description language and uses the existing automation tools which are specifically designed for synchronous implementation. This fact supposes a disadvantage when comparing performances, consumption and areas to a synchronous model, but it make possible to test and produce asynchronous circuits easily. We have designed an asynchronous adder implemented with the logic gates of our library and it has been successfully simulated with Xilinx Foundation F 3.1i software.